

```
01 LBL "MI/O" ;Matrix Input/Output
02 FS? 00
03 CF 21
04 CLA
05 ARCL 04
06 >" MATRIX"
07 AVIEW
08 ADV
09 LBL 00
10 RCL 02
11 STO 00
12 FIX 0
13 ADV
14 "ROW "
15 ARCL 01
16 >":" ;Append 1 colon
17 AVIEW
18 LBL 01
19 CLA
20 FIX 1
21 RCL 01
22 INT
23 RCL 00
24 E2
25 /
26 +
27 RCL 01
28 RCL 00
29 XROM 20,36 ;M5 - PPC ROM Matrix, (i,j) to Register Address
30 CF 28
31 ARCL 03
32 >"\28" ;Append left parenthesis
33 ARCL Y
34 SF 28
35 FS? 00
36 GTO 02
37 >"\29=" ;Append right parenthesis, equal sign
38 RCL IND X
39 FIX 4
40 ARCL X
41 AVIEW
42 GTO 03
43 LBL 02
44 >"\29?" ;Append right parenthesis, question mark
45 PROMPT
46 STO IND Y
47 LBL 03
48 ISG 00
49 GTO 01
50 ISG 01
51 GTO 00
52 CF 00
53 FS? 55
54 SF 21
55 END
```

0070C000F5004D492F4FAC00A915879B04F87F204D41545249
587E8F0122309C008FF4524F57209B01F27F3A7E02879C0121
68201B1243402120A524A91C9B03F27F289B72A81CAC00B300
F37F293D90F39C049B737EB40003F37F293F8E91F2049600B2
009601B100A900AC37A815C0000D19

112 BYTES

HP-41C Matrix Input/Output by John H. Nickel PPC V9 N5 P17 Aug. 1982

Program Registers Needed: 16

Row 1 (1 - 4)



Row 2 (5 - 8)



Row 3 (9 - 15)



Row 4 (16 - 24)



Row 5 (25 - 32)



Row 6 (33 - 38)



Row 7 (38 - 44)



Row 8 (45 - 52)



Row 9 (52 - 55)

